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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,429	02/16/2000	Takao Toi	Q57908	7134

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EXAMINER
LAROSE, COLIN M

ART UNIT	PAPER NUMBER
2623	7

DATE MAILED: 05/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/505,429	TOI, TAKAO	
	Examiner	Art Unit	
	Colin M. LaRose	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Arguments and Amendments

1. Applicants' arguments and/or amendments filed 18 March 2003, have been entered and made of record.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 16 February 2002 has been considered by the examiner.

Response to Amendments and Arguments

3. Applicant's arguments with respect to claim 1 have been fully considered but they are not persuasive for at least the following reasons.

Applicant asserts that Kolchinsky's host processor (14) of figure 8 and camera head (12) of figure 9 are separate and unrelated embodiments. However, figure 1 shows the two components used together in combination in the same system and connected by cable 13. The processor 70 of the camera head 12 provides control functions (column 7, lines 44-48). The processor 66 of the host processor 14 provides digital signal processing of the image captured by the camera (column 7, lines 12-33). Thus Baxter discloses both control and image signal processing in a single embodiment albeit in separate hardware components. Kolchinsky is relied upon for the teaching that separate image and control processors are advantageously combined into a single reconfigurable processor that utilizes FPGAs.

Kolchinsky, column 1, lines 16-29:

Conventionally, different imaging/control operations require "separate hardware implementations in separate boards or separate gate arrays," which is inefficient and expensive.

Kolchinsky, column 1, line 56 through column 2, line 2:

An object of Kolchinsky's system is to provide a single processor comprised of reconfigurable gate arrays such that the single processor is reconfigurable to perform different operations on image data and such that "the processing algorithm can be changed easily and quickly without hardware replacement."

Essentially, Kolchinsky's reconfigurable processor (12, figure 1) replaces the separate processors (66 and 70) of Baxter. Figure 4 of Kolchinsky shows that the single processor is operative perform both control (zooming/panning) and image (color processing, image compression) processing.

Claim 1 calls for an image processing system provided with a field programmable gate array capable of altering the logic description describing an operating state but does not preclude the presence of a second FPGA. Kolchinsky teaches that for image/control processing, FPGA 22 (figure 2) selects the addresses of the image data from the image bank 24 to be processed; the image data is then supplied to FPGA 26 for processing (column 3, lines 23-27). Thus, FPGA 26 executes the image and control processing and FPGA 22 performs addressing operations.

Applicant argues that the combination of Baxter and Kolchinsky is invalid because Baxter relates to video processing using specialized hardware and Kolchinsky relates to reconfigurable sequential processors and programmable gate arrays for use in general-purpose

computers, and Kolchinsky does not teach or suggest that FPGAs can be used with the analog video cameras of Baxter.

However, both references are closely related to systems for image acquisition and processing. Kolchinsky teaches utilizing a single processor to perform the image and control processing functions of multiple processors, such as those (66 and 70) disclosed by Baxter. One skilled in the art would have motivated to replace Baxter's processor 70 used to control the video camera with Kolchinsky's single processor 12 and therefore, would have known that the processor comprised of FPGAs is used with the analog camera of Baxter.

Also, applicant argues that the combination of Baxter and Kolchinsky would require extensive redesign, experimentation, and testing in order to achieve the claimed invention, there is no suggestion to motivate a combination, and neither reference discloses how the combination would be accomplished. However, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, the teachings of Kolchinsky are relied upon to demonstrate that multiple processors performing multiple functions of image and control processing are preferably replaced by a single reconfigurable processor comprising FPGAs, wherein the single processor is operative to perform the same functions as the multiple processors.

4. With regards to the argument that Fukuoka is non-analogous art and therefore is invalid, both Fukuoka (column 1, lines 19-22) and Baxter (title) relate to the interfacing of an electronic camera.

Newly added claims 11-20 recite features analogous to those of claims 1-10, respectively. The above remarks for claims 1, 5, and 6 apply to claims 11, 15, and 16 as well.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-4, 7-10, 11-14, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,486,853 by Baxter et al. ("Baxter") and U.S. Patent 5,301,344 by Kolchinsky.

Regarding claims 1 and 11, Baxter discloses an image processing system (figures 8 and 9), an image processing method of the system comprising:

executing digital image processing of interval of active pixel by processor 66 (figure 8) to perform various functions on pixel data (column 7, lines 18-31: automatic gain control, luminance derivation, etc.);

executing digital control processing according to commands issued during an interval of non-active pixel (i.e. during blanking periods); [Column 7, lines 48-55: control commands are received by processor 70 during blanking period and executed accordingly.]

executing digital image processing again (each line of an image constitutes a different active/non-active region, so digital image processing is repeated for every said region in order to process an entire image).

Baxter is silent to utilizing an FPGA for executing said image and control processing wherein first and second internal logic descriptions, corresponding to each processing, are written to the FPGA. Instead, Baxter teaches utilizing dedicated processors 66 and 70 for executing each type processing.

Kolchinsky discloses a reconfigurable image processing system (figure 2) that is implemented by FPGAs (22 and 26, figure 2), wherein arithmetic unit 26 is operative to process image data. Kolchinsky teaches that, conventionally, separate image processing operations require separate hardware (column 1, lines 23-24). Baxter, as noted above, requires separate processors (66, figure 8, and 70, figure 9) for image processing and control processing.

Kolchinsky's system uses reconfigurable gate arrays to perform a variety of operations, so that processing algorithms "can be changed easily and quickly without hardware replacement" (column 2, lines 1-2). That is, the functions of multiple dedicated processors such as those taught by Baxter are be performed by a single reconfigurable processor disclosed by Kolchinsky.

With reference to figure 3, first, the command corresponding to the operation to be executed is read from the command file at step 50. Then, the code corresponding to the operation is identified and placed into a register at step 52. Then, the command is executed at step 58 on the condition that proper reconfiguration of internal logic has occurred.

Kolchinsky teaches (figure 4) that both image processing (e.g. image compression, color processing) and control processing (e.g. zooming/panning) are executed by the system.

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace Baxter's separate processors 66 and 70 by Kolchinsky's reconfigurable FPGAs to achieve the claimed invention since Kolchinksy provides a much simpler and more hardware-efficient system for effecting image and control processing.

Regarding claims 2 and 12, Baxter teaches there is provided an image pick-up element (CCD 22, figure 9), the system executing color signal processing during active pixel interval and control processing during non-active interval, as addressed above for claim 1.

Regarding claims 3 and 13, Baxter teaches interval of non-active pixel is a VBI (column 7, lines 48-51).

Regarding claims 4, 7, 14, and 17, Baxter does not expressly disclose utilizing the HBI and optical black pixel interval as non-active regions, however, effecting control processing during the HBI and optical black pixel intervals was well-known by those skilled in the art and was a common practice at the time the invention was made. Official notice taken.

Regarding claims 8-10 and 18-20 Baxter (column 7, lines 18-31) and Kolchinsky (figure 4) disclose performing white balance, AF, and lightness control processing.

7. Claims 5, 6, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter and Kolchinsky, and further in view of U.S. Patent 5,754,227 by Fukuoka.

Regarding claims 5, 6, 15, and 16, Baxter (column 7, lines 40-43) and Kolchinsky (figure 4) teach executing compression but do not expressly disclose executing control processing, such as code quantity control, in relation to the image compression in the non-active interval.

Fukuoka discloses a camera interface similar to that of Baxter wherein control commands are issued during the non-active interval (column 8, lines 40-43). Fukuoka also teaches performing compression on the active part of the image and teaches that control commands sent during the non-active interval comprise compression parameters, such as a scale factor, or code quantity (column 10, lines 7-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Baxter and Kolchinsky by Fukuoka to achieve the claimed invention since the ability to adjust the compression ratios and scale factors, as taught by Fukuoka, provides control over the compression operations.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colin M. LaRose whose telephone number is (703) 306-3489. The examiner can normally be reached Monday through Thursday from 8:00 to 5:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au, can be reached on (703) 308-6604. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2600 Customer Service Office whose telephone number is (703) 306-0377.

AMELIA M. AU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

CML
Group Art Unit 2623
6 May 2003